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EXAMINER	
CONTINO, PAUL F	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/689,408	CHEN, KER-MIN	
	Examiner	Art Unit	
	Paul Contino	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action: Non-Final Rejection

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 10-16 and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As in claims 10, 15, and 18, the Applicant claims respective limitations involving sampling of a test signal and then outputting that [sampled] test signal for conversion using a USB protocol. For example, claim 10 states "sampling the test signal and outputting the test signal ... converting the test signal to USB protocol". However, the Applicant's Specification and figure illustrations disclose sampling of a test signal and conversion of a test signal using USB protocol to occur separately *(Figs. 3,4; page 9)*. The Examiner recommends that the limitations differentiate between an "original" test signal and a "sampled" test signal. Claims 11-14 and 16 are rejected based upon their respective dependencies to claims 10 and 15.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 and 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takinosawa (U.S. Patent No. 6,977,960) in view of Mak et al. (U.S. Patent No. 6,885,209).

As in claim 1, Takinosawa teaches of a USB interface *(Figs. 1,2)*, comprising:

a test signal generator for generating a test signal *(Fig. 2 #35; column 5 lines 64-67, where BIST 35 generates a test signal)*;

a transmitter and a receiver coupled to a signal for accessing data at transmission terminals *(Fig. 2 #s 31,32; column 6 lines 31-48)*;

a USB transceiver macrocell coupled to the test signal coupled to the test signal generator, the transmitter, and receiver *(Figs. 1,2; columns 3 and 4, where USB transceiver macrocell 17 is coupled to the generator, transmitter, and receiver)*, the USB transceiver macrocell for converting the test signal with USB protocol, outputting a first converted signal through the transmitter, receiving the first converted signal through the transmission terminals and the receiver, and converting the received first converted signal to a second converted signal

(Fig. 2 #s 31,32,33; column 6 lines 31-48, where the conversion of the test signal is inherently done using a USB protocol); and

a comparator coupled to the USB transceiver macrocell and the signal sampling device for comparing the second converted signal with [a] test signal, and outputting an error-acknowledging signal *(Fig. 2 #49; column 6 lines 49-61 and column 7)*.

However, Takinosawa fails to teach of a signal sampling device. Mak et al. teaches of a signal sampling device coupled to the test signal generator for sampling the test signal and outputting the sampled test signal after a predetermined time *(Fig. 4; column 5 lines 6-22, where the latency adjuster 150 stores the test signal, holds the data for a latency period, and then releases the data again after that time – i.e. the data is sampled and released after a predetermined amount of time)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the sampling and delay as taught by Mak et al. in the invention of Takinosawa. This would have been obvious because holding, sampling, and releasing data as taught by Mak et al. allows for proper comparison of data to determine if an error has occurred in transmission *(column 5 lines 6-22)*.

As in claim 2, Takinosawa and Mak et al. teach the predetermined time is set according to the USB protocol implanted by the USB transceiver macrocell *(Mak et al.: column 5 lines 6-22; Takinosawa: Figs. 3,4a,4b; column 5 line 51 through column 6 line 61, where various control signals are present during the testing phase. Because the delay/sampling circuit is present within the USB device itself, a USB protocol must set the predetermined time)*.

As in claim 3, Mak et al. teaches the signal sampling device further comprising:

a memory for storing the test signal *(Fig. 4 #150; column 5 lines 6-22, where it is inherent that the test signal is stored in a memory in order to facilitate the latency)*; and

a delay device for delaying the test signal for the predetermined time, and outputting the test signal from the memory *(Fig. 4 #150; column 5 lines 6-22)*.

As in claim 4, Takinosawa teaches the test signal and the second converted signal are parallel signals *(Figs. 1,2 #s 21,25; column 4 lines 2-4, test signal 21, and column 4 lines 22-24, second converted signal 25)*.

As in claim 5, Takinosawa teaches that the first converted signal is a serial signal *(Figs. 1,2; column 4 lines 15-17 and column 5 lines 16-17, where the transceiver transmits/receives a first converted serial signal)*.

As in claim 6, Takinosawa teaches the USB transceiver macrocell converts the parallel test signal to the serial first converted signal, and converts the first converted signal received by the receiver to the parallel second converted signal *(Figs. 1,2; columns 4-6)*.

As in claim 7, Takinosawa teaches the comparator further comprises an enable terminal and is enabled when the enable terminal receives a testing enable signal representing the test of

the physical layer of the USB interface is performed *(Figs. 2,4b; column 7 lines 41-65, testing enable signal Compare Enable)*.

As in claim 10, Takinosawa teaches a testing method for a USB interface *(Figs. 1,2)*, comprising the following steps:

providing a test signal to a USB transceiver macrocell *(Fig. 2 #35; column 5 lines 64-67, where BIST 35 generates a test signal)*;

converting the test signal to USB protocol, outputting a first converted signal through a transmitter, receiving the first converted signal through a receiver, and converting the received first converted signal to a second converted signal *(Fig. 2 #s 31,32,33; column 6 lines 31-48, where the conversion of the test signal is inherently done using a USB protocol)*; and

comparing the second converted signal with [a] test signal and then outputting an error-acknowledging signal *(Fig. 2 #49; column 6 lines 49-61 and column 7)*.

However, Takinosawa fails to teach of a sampling a signal. Mak et al. teaches of sampling the test signal and outputting the test signal after a predetermined time *(Fig. 4; column 5 lines 6-22, where the latency adjuster 150 stores the test signal, holds the data for a latency period, and then releases the data again after that time – i.e. the data is sampled and released after a predetermined amount of time)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the sampling and delay as taught by Mak et al. in the invention of Takinosawa. This would have been obvious because holding, sampling, and releasing data as

taught by Mak et al. allows for proper comparison of data to determine if an error has occurred in transmission *(column 5 lines 6-22)*.

As in claim 11, Takinosawa and Mak et al. teach the predetermined time is set according to the USB protocol implanted by the USB transceiver macrocell *(Mak et al.: column 5 lines 6-22; Takinosawa: Figs. 3,4a,4b; column 5 line 51 through column 6 line 61, where various control signals are present during the testing phase. Because the delay/sampling circuit is present within the USB device itself, a USB protocol must set the predetermined time)*.

As in claim 12, Takinosawa teaches the test signal and the second converted signal are parallel signals *(Figs. 1,2 #s 21,25; column 4 lines 2-4, test signal 21, and column 4 lines 22-24, second converted signal 25)*.

As in claim 13, Takinosawa teaches that the first converted signal is a serial signal *(Figs. 1,2; column 4 lines 15-17 and column 5 lines 16-17, where the transceiver transmits/receives a first converted serial signal)*.

As in claim 14, Takinosawa teaches the USB transceiver macrocell converts the parallel test signal to the serial first converted signal, and converts the first converted signal received by the receiver to the parallel second converted signal *(Figs. 1,2; columns 4-6)*.

As in claim 15, Takinosawa teaches a testing method for a USB transceiver macrocell *(Figs. 1,2)*, comprising the following steps:

providing a test signal to the USB transceiver macrocell *(Fig. 2 #35; column 5 lines 64-67, where BIST 35 generates a test signal)*;

converting the test signal with a USB protocol and outputting a converted signal by the USB transceiver macrocell *(Fig. 2 #s 31,32,33; column 6 lines 31-48, where the conversion of the test signal is inherently done using a USB protocol)*; and

comparing the converted signal with [a] test signal and then outputting an error-acknowledging signal *(Fig. 2 #49; column 6 lines 49-61 and column 7)*.

However, Takinosawa fails to teach of a sampling a signal. Mak et al. teaches of sampling the test signal and outputting the test signal after a predetermined time *(Fig. 4; column 5 lines 6-22, where the latency adjuster 150 stores the test signal, holds the data for a latency period, and then releases the data again after that time – i.e. the data is sampled and released after a predetermined amount of time)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the sampling and delay as taught by Mak et al. in the invention of Takinosawa. This would have been obvious because holding, sampling, and releasing data as taught by Mak et al. allows for proper comparison of data to determine if an error has occurred in transmission *(column 5 lines 6-22)*.

As in claim 16, Takinosawa and Mak et al. teach the predetermined time is set according to the USB protocol implanted by the USB transceiver macrocell *(Mak et al.: column 5 lines 6-*

22; Takinosawa: Figs. 3,4a,4b; column 5 line 51 through column 6 line 61, where various control signals are present during the testing phase. Because the delay/sampling circuit is present within the USB device itself, a USB protocol must set the predetermined time).

As in claim 17, Takinosawa teaches a USB interface *(Figs. 1,2)*, comprising:

a test signal generator for generating a test signal *(Fig. 2 #35; column 5 lines 64-67, where BIST 35 generates a test signal)*;

a USB converter logic coupled to the test signal generator *(Figs. 1,2; columns 3 and 4, where USB transceiver macrocell 17 is coupled to the generator)*, the USB converter logic including logic for converting the test signal into a USB protocol signal, circuitry for receiving the USB protocol signal and looping the signal back to the USB converter logic *(Fig. 2 #s 31,32,33; column 6 lines 31-48, where the conversion of the test signal is inherently done using a USB protocol)*;

logic within the USB converter circuit for converting the loop-backed signal into a loop-backed converted signal having a protocol comparable to the test signal *(Fig. 2 #s 31,32,33; column 6 lines 31-48, where the conversion of the test signal is inherently done using a USB protocol)*; and

a comparator coupled to the USB converter circuit, the comparator configured to compare the loop-backed converted signal with the delayed test signal *(Fig. 2 #49; column 6 lines 49-61 and column 7).*

However, Takinosawa fails to teach of delay logic. Mak et al. teaches of delay logic *(Fig. 4; column 5 lines 6-22, where the latency adjuster 150 is delay logic).*

It would have been obvious to a person skilled in the art at the time the invention was made to have included the delay logic as taught by Mak et al. in the invention of Takinosawa. This would have been obvious because delaying data as taught by Mak et al. allows for proper comparison of data to determine if an error has occurred in transmission *(column 5 lines 6-22)*.

As in claim 18, Takinosawa teaches a testing method for a USB transceiver *(Figs. 1,2)*, comprising:

providing a test signal to a USB signal converter *(Fig. 2 #35; column 5 lines 64-67, where BIST 35 generates a test signal)*;

converting the test signal with a USB protocol and outputting a converted signal by the USB signal converter *(Fig. 2 #s 31,32,33; column 6 lines 31-48, where the conversion of the test signal is inherently done using a USB protocol)*; and

comparing the converted signal with [a] test signal and then outputting an error-acknowledging signal *(Fig. 2 #49; column 6 lines 49-61 and column 7)*.

However, Takinosawa fails to teach of a sampling a signal. Mak et al. teaches of sampling the test signal and outputting the test signal after a predetermined time *(Fig. 4; column 5 lines 6-22, where the latency adjuster 150 stores the test signal, holds the data for a latency period, and then releases the data again after that time – i.e. the data is sampled and released after a predetermined amount of time)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the sampling and delay as taught by Mak et al. in the invention of Takinosawa. This would have been obvious because holding, sampling, and releasing data as

taught by Mak et al. allows for proper comparison of data to determine if an error has occurred in transmission *(column 5 lines 6-22)*.

* * *

1. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takinosawa in view of Mak et al., further in view of AAPA (Applicant's Admitted Prior Art).

As in claim 8, the combined invention of Takinosawa and Mak et al. teaches of a USB serial interface *(Takinosawa: Fig. 1; column 3 lines 45-46)*. However, the combined invention of Takinosawa and Mak et al. fails to teach of a serial interface engine containing a USB packet ID and address recognition logic, sequencing and state machine logic to handle USB packets and transactions. AAPA teaches of these elements *(Fig. 1; Specification pages 1-2)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the elements as taught by AAPA in the serial interface of the combined invention of Takinosawa and Mak et al. This would have been obvious because the described elements are inherent to a USB 2.0 interface such as that in the combined invention of Takinosawa and Mak et al. *(Takinosawa: Fig. 1)*.

As in claim 9, Takinosawa teaches the testing enable signal is output by the serial interface engine or controlled externally from USB transceiver macrocell *(Figs. 1,2,4b; column 3 line 45 through column 4 line 18)*.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent 6,023,774 Minagawa discloses loopback testing of a transmission device.

U.S. Patent 6,816,988 Barford discloses comparing a delayed signal with a DUT signal.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PFC
12/18/2007

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER